RAVI LAKKAPPA BELLUBBI

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EDUCATION

Master of Science - Computer Engineering (Specialization: VLSI & Computer Architecture); GPA : 3.53 08/2023 – 05/2025
The George Washington University Washington DC, USA

Bachelor of Engineering - Electronics and Communication; CGPA : 7.73, Major GPA : 8.54 2018 – 2022
Dayananda Sagar College of Engineering Bangalore, India

SKILLS

OS, EDA, FPGA & CPLD Tools
Linux, Cadence - Xcelium, Virtuoso, Voltus & Innovus, Tetramax, QuestaSim, Makerchip, MPLAB X IDE, Quartus prime, Synopsys VCS, LT Spice, H Spice, WinMIPS64, Dinero, Scale-sim, Booksim2, Gem5

Hardware, Scripting & Assembly Languages
C, C++, C#, Verilog, TL-Verilog, System Verilog, VHDL, Nios ii, MATLAB, Simulink, Python, Perl, TCL, Bash, Makefile, Git, Git version control and Assembly language

Protocols, Peripheral Controllers and Interfaces
Ethernet, PCI, PCIe, UART, AMBA, I2C, SPI, APB, AHB, AXI

System Architectures
ASIC, FPGA, Memory, SoC, CPU, GPU, O-RAN

WORK EXPERIENCE

Trainee Intern - FPGA Design and Verification Engineer 06/2024 – 08/2024
Akkodis Kings of Prussia, USA

- *Verified PCIe IP components (DLL Transmitter/Receiver, Replay Buffer etc.) using UVM testbenches in QuestaSim, while optimizing low-power RTL coding for the PCIe DLL layer and assisting with synthesis, timing closure, and FPGA prototyping.*
- *Developed formal verification methods for AHB2APB bridge and contributed to chip-level verification.*
- *Performed FPGA design verification using Cadence Innovus, generated coverage reports in QuestaSim, conducted ATGP with Synopsys VCS, and automated testbench setup using Perl/Python, makefile scripting improving test efficiency.*

Trainee Intern - Verification Engineer 07/2022 – 02/2023
Velodyne Lidar India Pvt. Ltd Bangalore, India

- *Debugged Velarray M1600 by analyzing waveforms and understanding real-time testbench programming.*
- *Verified the scanner block in the Condor project by integrating MATLAB functions with SystemVerilog DPI-C, utilizing the Octave library in C/C++.*
- *Tested Lidar peripherals (top & bottom board) in the Next-Generation Platform project, gaining experience with MPLAB X IDE, IPE, Cheetah SPI host adapter, and Saleae Logic Analyzer.*

Trainee - Advanced VLSI Design & Verification 02/2022 – 08/2023
Maven Silicon Bangalore, India

- *Excelled skills in the domains of DFT, FPGA Design, STA & Verification Methodologies such as OVM, UVM and Assertion based Verification: SVA.*
- *Developed projects such as Router 1×3 and AHB2APB Bridge Verification.*

PROJECTS

AES Encryption Core 03/2025
The George Washington University

- *Designed and implemented an AES-128 encryption core in Verilog, utilizing a 10-round pipelined architecture with SubBytes, ShiftRows, MixColumns, and AddRoundKey transformations for high-throughput encryption.*
- *Optimized FPGA resource utilization through register retiming and logic balancing, improving area and power efficiency.*
- *Performed synthesis, back-annotation, and layout analysis, generating STA reports for timing closure, area, and clock performance.*
- *Verified the design using Tmax ATPG for fault coverage analysis, conducted functional and gate-level simulations, and generated coverage reports to validate correctness.*

Machine Learning for Optimized Computer Architecture Designs 12/2024
The George Washington University

- *Adjusted computer architecture parameters such as cache size, core frequency, voltage etc. for better performance, power efficiency, and reliability for CNN algorithm Accelerator*
- *Utilized Aladdin Gem5 and Smaug to evaluate area, power, execution time, energy consumption, and reliability, with my proposed architecture outperforming traditional heuristics by adapting to workloads.*

64-QAM modulator 12/2023
The George Washington University

- *Implemented a 64-bit QAM Modulator with SPI, Symbol Mapping, CDC FIFO, and Data Register blocks, capable of processing a 60 Mbit/sec datastream and storing data at 10 MHz.*
- *Performed synthesis, back-annotation, and layout, generating reports for timing, area, and clock performance. Verfied the design using Tmax tool and generated coverage reports*

AHB2APB Bridge IP Core – Design & Verification 02/2023
Maven Silicon

- *Designed the AHB-to-APB Bridge IP in Verilog by developing the micro-architecture and implementing pipelined AHB-slave logic with correct protocol conversion to the non-pipelined APB interface.*
- *Developed RTL for address phase, data phase, and handshake logic; validated single and burst read/write transfers using self-checking testbenches.*
- *Built a UVM-based verification environment, creating directed + constrained-random sequences to verify protocol conversion, wait-state behavior, response signaling, and peripheral selection.*
- *Implemented functional coverage models for AHB/APB transactions and achieved coverage closure and RTL sign-off through simulation, synthesis checks, and code-coverage analysis.*